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EXAMINER	
FLEMING, FRITZ M	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 09/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/851,169	THOMAS ET AL.	
	Examiner	Art Unit	
	Fritz M Fleming	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-43 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-43 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
PRIMARY EXAMINER
GROUP 2100

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2,6.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 26 rejected under 35 U.S.C. 102(b) as being clearly anticipated by Ishigure.

The claim as presently drafted is clearly anticipated due to the following:

- A switchable processing element at refresh controller 4 as it has its speeds switched,
- A first port at either 10 or 11 accepting either 7 or 8, or 12 or 9, respectively, to constitute a first clock signal as 7,8,9,12 are all clock oscillators, thereby producing clock signals,
- A second port at either 10 or 11 accepting the other of 7 or 8, or 12 or 9, respectively, to constitute the second other clock signal,
- A switch operable as shown in 10 or 11 between two modes to select either of 7/8 or 9/12, respectively, under the control of switching register 13,
- Wherein the selected clock signal is provided to controller 4.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 43 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The exact metes and bounds of the claim are not clearly discernable, hence rendering the claim vague and indefinite. First of all, there are two instances of "within the within" which is simply unclear. The language makes it unclear if a single clock input and output conductor are claimed per each individual processing element, or if there is just a single one of each for the entire macro. The remaining specifics of the claim are vague and indefinite as relationships such as "increased length", "decreased length", "adjacently placed", "space efficient" and the like are simply not defined in the specification to give proper interpretational bounds to these terms of relative degree.

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claim 43 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the

time the application was filed, had possession of the claimed invention. Besides a literal copy of the claim to provide literal antecedent basis for what is claimed, the specification provides no guidance as to the specifics of the claim. For example, a quite detailed and intricate layout structure is claimed, involving numerous conductors, while the specification does not address such specifics. A careful reading of the specification reveals that there is no definition of what is to be construed by "space efficient" or the increased or decreased lengths of the various conductors, with the various conductors not adequately defined or described either. In order to overcome this rejection, it is clear that the specification must show (with a reference numeral) and clearly describe each and every feature of the claim, all without the prohibited addition of "new matter", thus requiring a showing of where each amendment to the specification/drawings finds support in what was originally filed. Absent a clear meaning to be ascribed to the various terms and elements, a rejection based on art is presented as best as the claim can be understood.

7. Claim 43 is rejected under 35 U.S.C. 102(b) as being anticipated by Amdahl.

Given the best interpretation possible, supra, Amdahl appears to disclose what the claim seems to be directed to. Note that the chips (i.e. A-C) are arranged serially such that the clock at 218 enters an input at 222 or 242, and then proceeds serially at "a" to 232/252, and then to "a"/"b" and then serially to 246/256 and 236/226 and then serially to the ultimate destination at 254/244/224/234. Each chip broadly meets a "processing element" as chips

perform processing functions, and each broadly meets a "macro" wherein the "macros" are arranged in a "space efficient manner" per the Figures such that they interconnected, with the goal of equalization via delay paths. Per column 5, lines 28+, chip interconnection is to include transmission lines of uniform impedance, delay per unit length and of equal length. Thus chips closer to the clock input source will have shorter paths than those located downstream, with ultimately equal delay paths the result. This would seem to cover delay equalization within the chips as well as chip to chip lengths.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any

inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

11. Claims 1,27,28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakakura in view of Janssens et al. (Janssens).

Nakakura discloses the invention substantially as claimed, for example, at Figures 3a/b. A pipelined processor is shown thus meeting serially connected processing elements up to an nth one, with a clock cycle going to latches 1,2,3 is delayed from latch 1 to 2, but latch 3 is the same timing as latch 1, thereby not meeting each subsequent delay. It is to be noted that per Figure 3b, a new data is clocked into latch 1 at every clock cycle, thereby meeting the claimed k=1. It is to be noted that the whole idea of Nakakura is to use a skew or delay (IV) in order to decrease the overall time needed by the pipeline. In fact, explicit mention is made at column 3, lines 22+, that the delay makes it possible to use a shorter cycle, thereby increasing the overall speed. Figure 5 shows that under conventional pipelining, the maximum processing time of 13 nanoseconds would have been used as the stage clock cycle, thereby representing the normally sufficient time. However, with the delay of 4 nanoseconds, a clock stage of 10 nanoseconds can be used, thereby shortening the cycle time to what would be a

value in which accurate output would not be possible, due to insufficient time. But with the delay, the time is sufficient for accurate outputs.

In the same art of delayed clocking to pipeline stages, Janssens teaches at Figure 1 a three stage apparatus with delayed clocks at 14 and 12b, compared to 12a, per Figure 2. The purpose is to speed throughput in the pipeline.

Thus it would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify Nakakura per the teachings of Janssens in order to have each subsequent processing element receive a delayed clock, when multiple slower elements are used, as Nakakura clearly teaches to use delays with the slower elements when it is desired to lower the overall cycle time below the slowest element. Clearly the criteria are given how to correctly calculate for multiple delays (i.e. each subsequent clock delayed per Janssens) while still speeding throughput by a lowered overall clock cycle.

12. Claims 2-11,29-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakakura in view of Janssens as applied to claims 1,27,28 above, and further in view of Molnar et al. (Molnar).

Nakakura in view of Janssens lack the first and second paths, with the second path being shorter than the first.

Molnar teaches the use of a counterflow pipeline, for use in asynchronous or synchronous applications of signal processing, associative memory, and computer architectures. Per Figure 1, 22 shows a flowing of data up/down the pipeline in forward and reverse flow, by means of a single data path 22 or

multiple paths 24 and 26. Control system 52 ensures orderly flow between the stages n-1, n and n+1 and so on.

Therefore it would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify Nakakura and Janssens by the teachings of Molnar so as to be able to use forward and reverse flow processing on the pipeline in a clock synchronized manner. As Molnar uses stage designation of n-1, n and n+1 and assuming that such is in the forward direction of the notation of Nakakura, then reverse flow processing would go in the order of n+1, n, and n-1 and thereby intrinsically take advantage of the shorter cycles at the rising edges of Nakakura and Janssens due to the delays in the forward direction, which result in a "speedup" in the reverse direction of n+1, n and n-1. Per Janssens, each delay is the same (i.e. 1/3 delay for the stages of Figure 1). The overall teachings show independent clock cycle delivery due to the delays at each subsequent element per Janssens. In order to flow forward and reverse, the clock would thus have to be selectable in its direction of propagation. Per the above, k=1. Per Nakakura, external time synchronization is to the clock 100. A memory buffer is taught by any of the latches shown. Janssens shows I/O ports at 8 and 9, respectively. Nakakura teaches the use of Figure 4 to cause the delay, such not including gating. However, it is notoriously well known in the art to use gating to cause equivalent delays, and the examiner takes official notice of such. Janssens shows the first external circuit at 8 to which the pipeline is synchronized in order to read in the data. While a memory is not explicitly taught for Janssens' initial circuit 8, such includes "data processing" which would

obviously include a memory of some kind in order to have the result be available for initial processing by the first register 12a upon the clocking. Likewise, the end element 9 would also have some kind of memory, as column 3, lines 39-43 include mention of registers in 8 and 9, thereby rendering obvious a "memory" at 8 and 9 as registers are a memory. The exact length of delay plus clock cycles is determined by the rate at which data is clocked in/out. However, given Nakamura's Figure 5, a 10 nanosecond cycle time is used with a 4 nanosecond delay, thus adding the two arrives at 14 nanoseconds, and a subtraction of the two yields 6 nanoseconds. Thus in the direction of the delay, such is longer (14) than the processing time of 13 nanoseconds required without the delay, and in the reverse direction (6), it is shorter than the direction of the delay (13) and longer than the opposite direction (i.e. 10-5=5). While 10 is not an exact average, such is ultimately determined by the speeds of the stages, with two slower speed stages working with one faster stage would result in a more average figure for the overall cycle time. While encryption is not specifically stated, such falls under the broad teachings of Molnar's applications, especially given applicants' admission that encryption is well suited for bidirectional pipelines such as Molnar's. As far as synchronization a the center is concerned, such is a function of the overall number of stages, and synchronization is ensured due to the use of the clocking schemes of the references.

13. Claims 12-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakakura, Janssens and Molnar as applied to claims 2-11,29-42 above, and further in view of Choe et al. (Choe).

Nakakura and Janssens and Molnar lack the two pipeline arrays.

Choe teaches the use of pipeline units 102 and 103each having a different number of stages, wherein the number of stages are determined by the operations of the pipelines, per column 5.

Therefore it would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify Nakakura, Janssens and Molnar per the teachings of Choe so as to be able to perform more complex pipeline operations such as reduction and addition. As for the numbers of stages in each pipeline, such depends on the operation to be performed per Choe. As shown in Choe, the first stage of 102 is 1021 and thus where the incoming data is first encountered. Thus applied to the other references, an electrical connection (i.e. hardwired) is needed at at least the stages, so as to ensure proper operations and synchronization. By calling 1025 the nth element, and 1031 the mth, the claimed subject matter is met. As the references require time synchronized delay based clocking, transfer from the n to mth element would also have the same delay per stage per Janssens. In a multi pipeline arrangement, all stages are in ultimate electrical communication with a memory buffer at 8 or 9 of Janssens. 1031 is the first stage of the second pipeline, wherein data from the nth stage 1025 is further processed. As far as adding a third pipeline in a serial manner of the other two of Choe, such is within the fair teachings of the combined references, as Janssens teach additionally clocked stages at 8 and 9 and Choe teaches the number of pipelines and stages dependent upon the computations to be performed. Thus the addition of a third pipeline in a similar

head to tail manner via a hardwired electrical connection is obvious subject matter, along with the number of stages of the third pipeline, as well as the synchronization and delays causing the clocked synchronization.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ido et al. Teach equalization. Wong et al. teach skew and serpentine lines 340-344 for skew matching. Mann teaches trace delay compensation. Ahuja teaches input delays. Jacobowitz et al. teach clock input and output at 122 and 151. Zelikson et al. And Kermani teaches distribution schemes. Nam teaches delayed clocks with an external clock and cell and data output. Duxbury et al. Teach pipelines. Lefsky et al. Teach clock skew avoidance. Nguyen et al. Teach pipelined data processing with delays serially inserted. Gunadisastra teaches the generation of a delayed clock based upon a gated clock.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fritz M Fleming whose telephone number is 703-308-1483. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin can be reached on 703-308-1483. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Fritz M Fleming
Primary Examiner
Art Unit 2182

fmf